출력 일자: 2003/2/25

발송번호 : 9-5-2003-006156434
발송일자 : 2003.02.24
제출기일 : 2003.04.24

수신 : 서울특별시 강남구 역삼동 648-1번지 BYC 빌딩 904호
이종일 귀하

135-080

특허청
의견제출통지서

출원인 명칭 가부시키가이샤 히타치세이사쿠쇼 (출원인코드: 519987107315)
주소 일본 도쿄토 치요다쿠 간다스루가다이 4쪼메 6반치

대리인 성명 이종일
주소 서울특별시 강남구 역삼동 648-1번지 BYC빌딩 904호

출원번호 10-2001-7004042

발명의 명칭 반도체장치

이 출원에 대한 심사결과 아래와 같은 거절이유가 있어 특허법 제63조의 규정에 의하여 이를 통지하오니 의견이 있거나 보정이 필요할 경우에는 상기 제출기일까지 의견서 또는/및 보정서를 제출하여 주시기 바랍니다. (상기 제출기일에 대하여 매회 1월 단위로 연장을 신청할 수 있으며, 이 신청에 대하여 별도의 기간연장승인통지는 하지 않습니다.)

[이 유]

이 출원의 특허청구범위 제 전항에 기재된 발명은 그 출원전에 이 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 아래에 지적한 것에 의하여 용이하게 발명할 수 있는 것이므로 특허법 제29조제2항의 규정에 의하여 특허를 받을 수 없습니다.

[아래]

본원 발명은 제 2 도전체막이 구리, 금, 백금 또는 상기 금속의 합금을 주성분으로 하고, 제 1 도전체막은 로듐, 르테늄, 이리듐, 오스뮴, 백금 중 하나를 주원소로 하면서 파라듐, 코발트, 니켈, 티탄 중 하나를 첨가원소로 하는 것을 주요특징으로 하는 반도체 장치에 관한 발명이나, 일본공개특허공보 평5-315336호(1993.11.26 공개)의 요약, 청구항1-4, 상세한설명 [0041]-[0044] 및 대표도와 일본공개특허공보 평10-229084호(1998.8.25 공개)의 요약 및 대표도에 상기 원소의를 주원소 또는 첨가원소로 이용하는 구성에 대한 기재가 있으므로, 본원 발명은 일본공개특허공보 평5-315336호(1993.11.26 공개) 및 일본공개특허공보 평10-229084호(1998.8.25 공개)의 공지기술에 의하여 용이하게 발명할 수 있습니다

[첨 부]

첨부 1 일본공개특허공보 평05-315336호(1993.11.26) 1부
첨부2 일본공개특허공보 평10-229084호(1998.08.25) 1부 끝.

2003.02.24

특허청 심사4국
반도체1심사담당관실 심사관 반성원

출력 일자: 2003/2/25

<<안내>>

문의사항이 있으시면 ☎ 042-481-5982 로 문의하시기 바랍니다.

특허청 직원 모두는 깨끗한 특허행정의 구현을 위하여 최선을 다하고 있습니다. 만일 업무처리과정에서 직원의 부조리행위가 있으면 신고하여 주시기 바랍니다.

▶ 홈페이지(www.kipo.go.kr)내 부조리신고센터

出力日付：2003/2/25

発送番号 ： 9－5－2003－006156434
発送日付 ：2003. 02. 24
提出期限 ：2003. 04. 24

宛て先 ：ソウル特別市江南区駅三洞 648－1
ＢＹＣ ビル 904 号
李 鍾 一 様
１３５－０８０

特許庁

意見提出通知書

出 願 人　氏名　株式会社日立製作所　（出願人コード：519987107315）
　　住所　日本国東京都千代田区神田駿河台４－６
代 理 人　氏名　李 鐘 一
　　住所　ソウル市江南区駅三洞 648－1 BYC ビル 904 号
出願番号　10－2001－7004042
発明の名称　半導体装置

本出願に対する審査結果、下記のように拒絶理由があって特許法第 63 条の規定に拠りそれを通知致しますので、もし意見があるか、補正が必要な場合には、前記提出期限までに意見書又は/及び補正書を提出して下さい。（前記提出期限に対する延長は、毎回１月単位で延長することができ、別途の期限延長承認の通知はしません．）

［理 由］

本出願の特許請求範囲第 全項に記載された発明は、その出願前にこの発明が属する技術分野において通常の知識を持つ者が下記に指摘したことにより容易に発明できるもので、特許法第 29 条第 2 項の規定により特許を受けることができません。

［下記］

本発明は第 2 導電体膜が銅、金、白金または前記金属の合金を主成分とし、第１導電体膜はロジウム、ルテニウム、イリジウム、オスミウム、白金のうち一つを主元素としながら、パラジウム、コバルト、ニッケル、チタンのうち一つを添加元素とすることを主要特徴とする半導体装置に関する発明であるが、日本公開特許公報平 5-315336 号(1993. 11. 26 公開)の要約、請求項１～４、詳細な説明［0041］～［0044］及び代表図と、日本公開特許公報平 10-229084 号(1998. 8. 25 公開)の要約及び代表図に前記元素を主元素または添加元素に用いる構成に対する記載があるので、本願発明は日本公開特許公報平 5-315336 号(1993. 11. 26 公開)及び 日本公開特許公報平 10-229084 号(1998. 8. 25 公開)の公示技術により容易に発明することができる。

［添付］

添付 1.　日本公開特許公報 平 05-315336 号(1993. 11. 26)　1 部
添付 2.　日本公開特許公報 平 10-229084 号(1998. 08. 25)　1 部　以上。

2003. 02. 24

特許庁　審査４局
半導体 1 審査担当官室

English Translation of Chinese Office Action

[Reason]

All the Claims of the present Chinese application can be invented easily by those skilled in the art, as indicated in the following Remarks below. So, the present application cannot be allowed by Chinese Patent Law Article 29(2).

[Remarks]

The present invention relates to the semiconductor device characterized mainly by the feature that the second conductive film includes copper, gold, platinum or alloy thereof as the main component, and the first conductive film includes one of rhodium, ruthenium, iridium, osmium and platinum as the main element, and one of palladium, cobalt, nickel and titanium is added as the additive. However, the constitution of the main element and the additive element are disclosed in Abstract, Claims 1-4, the descriptions of the specification Paragraphs [0041] – [0044] and the representative drawings of JP-A-5-315336 (published on November 26, 1993) and Abstract and the representative drawings of JP-A-10-229084 (published on August 25, 1998). So, the present invention can be invented easily from the prior arts disclosed in JP-A-5-315336 (published on November 26, 1993) and JP-A-10-229084 (published on August 25, 1998).

English Translation of Claims 1-4 of JP-A-5-315336

[Claim 1]

A method of fabricating a semiconductor device comprising the steps of;

forming a structure comprising a diffusion layer, a polysilicon layer or a metal-silicide layer formed on a semiconductor substrate, a first insulating film formed thereon and an inter-layers connection hole formed in said first insulating film, or forming a structure comprising a first insulating film formed on a semiconductor substrate, lower wiring constituted by one or plural layers of conductive films, a second insulating film formed on a first insulating film and an inter-layer connection hole formed in said second

insulating film;

forming a first conductive film layer of one layer or plural layers on said diffusion layer and said first insulating film, or on said lower wiring and said second insulating film;

forming a second conductive film layer on said first conductive layer;

forming a first mask film exposing only inside of said inter-layers connection hole and a surface of said second conductive film layer existing in periphery;

plating by using said first mask film as a plating mask and forming a first low-resistance metal film selectively on exposed said second conductive film layer;

removing said first mask film;

irradiating laser light to melt and reflow said first low-resistance metal film and filling said inside of said inter-layers connection hole with a material of said first low-resistance metal film;

forming thereon a third conductive film layer constituted by an element similar to an element of said second conductive film layer;

forming a second mask used for forming wiring, on said third conductive film layer, selectively;

plating by using said second mask as a plating mask, to form a second low-resistance metal film selectively on exposed said third conductive film layer;

removing said second mask film;

removing unnecessary portions of exposed said third conductive film layer, said second conductive film layer and said first conductive film layer in order to form metal wiring comprising said first conductive film layer, said second conductive film layer and said third conductive film layer; and

forming a third insulating film on said metal wiring.

[Claim 2]

A method of fabricating a semiconductor device according to Claim 1, wherein said first conductive film layer is formed by a single layer constituted by titanium (Ti), vanadium (V), zirconium (Zr), niobium (Nb), molybdenum (Mo), hafnium (Hf), tantalum (Ta), tungsten (W), alloy thereof, silicide thereof, nitride thereof, boride thereof and carbide thereof.

[Claim 3]

A method of fabricating a semiconductor device according to Claim 1, wherein said first conductive film layer is formed by two layers of titanium and titanium nitride or two layers of titanium and titanium boride.

[Claim 4]

A method of fabricating a semiconductor device according to Claim 1, wherein said second conductive film layer or said third conductive film layer is constituted by any one element or alloy of gold (Au), palladium (V), platinum (Pt), osmium (Os), iridium (Ir), rhodium (Rh), ruthenium (Ru), rhenium (Re), aluminum (Al) and copper (Cu).

English Translation of Paragraphs [0041] – [0044] of JP-A-5-315336

[0041] The first conductive film layer 105 performs as the adherence layer among the low-resistance metal film, the insulating film existing in the lower layer and the diffusion prevention film (barrier metal) which prevents the constituent element of the low-resistance metal film from diffusing and formed in the later process.

[0042] In addition, the high-melting temperature metals of zirconium, niobium, hafnium, vanadium and so on, alloy thereof, nitride thereof, carbide thereof, boride thereof, and the stacked layers of titanium and titanium nitride or titanium and titanium boride for attaining the heat proof and the adherence may be used except the materials described above.

[0043] The second conductive film layer 106 is formed for the purposes of forming the base for plating (the plating current providing layer), stabilizing the growth of the low-resistance metal film formed by plating, maintaining the adherence of the low-resistance metal film, and protecting the surface of the first conductive film layer 105 from the plating liquid.

[0044] Palladium, platinum, rhodium, osmium, iridium, ruthenium, and so on may be used. However, in principle, if the material is good at the heat-proof, the adherence and the plating as base for the growth of the first low-resistance metal film, the material is not limited to the elements described above. For example, the low-resistance metal film is constituted by copper or aluminum, copper or aluminum can be used as the second conductive film layer without causing problems.